REMARKS/ARGUMENTS

Claims 1-15 were pending in the application. By this amendment, claims 2, 6, 9, and 13 are being amended, and new claims 16-19 are being added, to advance the prosecution of the application. No new matter is involved. Reconsideration and allowance are respectfully requested.

In paragraph 1 on page 2 of the Office Action, claims 6 and 13 are objected to because "the oscillation circuit" is said not to have sufficient antecedent basis. In response, applicants are amending claims 6 and 13 to recite "an oscillation circuit" as suggested in the Office Action. Therefore, the basis for objection to claims 6 and 13 has been removed.

In paragraph 3 on page 2 of the Office Action, claims 2, 3, 9 and 10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. More specifically, the recitation "the input voltage" in claims 2 and 9 is said to have insufficient basis and is confusing with respect to the supply voltage. In response, applicants are correcting this recitation to state "the supply voltage", thereby clarifying the matter. As amended, claims 2 and 9, and claims 3 and 10 which depend therefrom, are now clear and definite.

In paragraph 5 on page 3 of the Office Action, claims 1 and 15 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,537,650 of West et al. In paragraph 7 on page 4 of the Office Action, claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over West in view of U.S. Patent 4,544,912 of Iwamoto et al. In paragraph 8 on page 5 of the Office Action, claims 2, 3, 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over West, or over West in view of Iwamoto as applied to claim 8, and further in view of U.S. Patent No. 6,297,622 of Yatabe. In paragraph 9 on page 7 of the Office Action, claims 4, 5, 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over West, or

over West in view of Iwamoto as applied to claim 8, and further in view of U.S. Patent No. 6,323,851 of Nakanishi. In paragraph 10 on page 10 of the Office Action, claims 6, 7, 13 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over West in view of Nakanishi as applied to claim 5, or over West in view of Iwamoto and further in view of Nakanishi, as applied to claim 12, and further in view of U.S. Patent 5,155,840 of Niijima. These rejections are respectfully traversed.

Briefly stated, the present invention provides a power supply circuit for a display device such as a liquid crystal. The circuit outputs a boosted supply voltage during normal operation, and generates a non-boosted supply voltage having a lower voltage than that during the normal display operation by controlling the switches for switching the output within the power supply circuit during a power save mode. The non-boosted supply voltage is supplied to the analog circuits of a driving circuit so that the power consumption at the analog circuit is reduced. By controlling the switch for switching the output within the power supply circuit and the supply of the power supply clock, the circuit can be switched, in the power save mode, to either a mode where a lower supply voltage is generated or to a mode where the supply is turned off.

Regarding the rejection of claims 1 and 15 as anticipated by West, it is noted that such reference only discloses that the power supply of a predetermined circuit is "switched off". That is, the reference discloses that a digital-to-analog converter circuit (DAC) is "shut-down" in, for example, a blanking period in order to reduce the power consumption, but fails to disclose actively "supplying", to a "digital-to-analog converter circuit" and an "analog signal processing circuit" of a driving apparatus for a display device, a "supply voltage" which allows the circuits to operate and which is lower than the voltage for the normal operation, as set forth in claims 1 and 15 of the present application.

It is a typical practice to switch the analog circuit off, as in West, in order to reduce the power consumption of the device. West, however, nowhere even suggests let alone discloses not switching the analog circuits off, or allowing the circuits to "operate" in conditions wherein the power consumption is to be reduced. Therefore, the invention defined in claims 1 and 15 cannot be expected from West, and there is no motivation in West to actively allow the analog circuits to "operate" during a "power save" as defined in the claims in accordance with the present invention. Therefore, claims 1 and 15 are submitted to clearly distinguish patentably over West.

Claims 2-14, which depend directly or indirectly from claim 1, are rejected as unpatentable over West in combination with other references such as Iwamoto, Yatabe, Nakanishi and Niijima. These claims contain all of the limitations of claim 1 so as to patentably distinguish over the basic reference of West. In addition, such dependent claims set forth additional limitations which distinguish patentably over the secondary references. This is discussed below.

Regarding U.S. Patent 6,297,622 of Yatabe, such patent has a U.S. filing date of September 15, 2000. The present application, on the other hand, has a priority date of March 31, 2000 which precedes the September 15, 2000 U.S. filing date of Yatabe. Therefore, Yatabe is not a proper reference against the present application. To prefect the priority claim, applicants are enclosing an English translation of Japanese Patent Application No. 2000-099890 on which the priority claim for the present application is based.

Regarding the Iwamoto reference, such reference is said to teach a digital-to-analog converter circuit that includes a plurality of voltage dividing resistive elements connected in series to the power supply from the power supply circuit, dividing the supply voltage into a plurality of stages by the voltage dividing resistance elements, and selecting a divided voltage corresponding to the digital

data, and outputting an analog signal. According to the Office Action, it would have been obvious to one ordinary skill in the art at the time of the invention to combine the digital-to-analog converter as taught by Iwamoto with the driving apparatus as taught by West.

However, a review of Iwamoto shows that it simply discloses a digital-to-analog converter. It fails to disclose or even suggest operation of the DAC during power save or the need for operating the DAC during power save. Therefore, the claims are not obvious over West in combination with the teaching of Iwamoto.

Regarding the Nakanishi reference, this reference is combined with West alone or in combination with Iwamoto. Nakanishi is said to teach a power supply circuit that comprises a boosting section for boosting the input voltage, a boosted power supply output switch for controlling passage between the boosting section and the output end of the power supply, and a non-boosted power supply output switch for bypassing the input and the output ends of the power supply. According to the Office Action, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the power supply circuit taught by Nakanishi with the driving apparatus taught by West or West in view of Iwamoto so that the two types of output switches are switched and controlled such that one of the boosted or non-boosted supply voltages is output to the digital-to-analog converter circuit and to the analog signal processing circuit.

Thus, the Office Action points out that the power supply circuit disclosed in Nakanishi outputs a non-boosted voltage by a voltage SW9 bypassing an input end and an output end of a power supply. In Nakanishi, when a "power supply is switched off" and the power supply voltage VDD is reduced, the switch SW9 is switched on and sets the output V0 to VSS (ground potential). However, Nakanishi also discloses that when this switch SW9 is switched on and the output V0 becomes VSS, switches SW1-SW8 are also switched on and the output voltages V1-V4, VO

and VDD from a power supply circuit 21 of Fig. 2 are all set to a ground potential. While it is true that this ground potential differs from a voltage boosted from the power supply voltage VDD supplied to the power supply circuit 21 during normal operation, Nakanishi discloses that when all of the output voltage is set to a ground potential VSS, the liquid crystal display element 10 to which the output voltage is supplied "does not emit light". This clearly indicates that no voltage is applied to a liquid crystal layer 15 positioned between a scan electrode 13 and a signal electrode 11, and that the liquid crystal display element 10 "cannot display". In addition, in Nakanishi, the liquid crystal display element 10 is actively "switched off" when the power supply is switched off, in order to prevent generation of an abnormal display when display is stopped.

The present invention is directed to "not switch the display off" during power save, and thus it is clear that the present invention is based on an idea opposite to that of Nakanishi. Moreover, Nakanishi only discloses that the liquid crystal display element 10 is switched off when the power supply is switched off, and fails to even suggest a state of "power save" in which the power supply is not switched off. Nakanishi also fails to even conceive how the display is to be controlled during a power save.

As described above, none of the references suggest a necessity for "displaying" while the power consumption is reduced by reducing the power supply voltage of analog circuits and not adjusting the operational clock during power save. Therefore, a driving apparatus in accordance with the present invention cannot be viewed as being obvious by combining Nakanishi and other references.

Similar comments apply to Niijima which is said to teach a clock for generating signals from an oscillation circuit. Again, the other references in combination therewith do not show or suggest the combinations of elements set forth in the claims.

Therefore, claims 1-15 are submitted to clearly distinguish patentably over the cited references.

With regard to new claims 16-19, independent claims 16 and 18 are similar to claims 1 and 15 except that the supply voltage is more restrictively defined. A basis for this more restrictive definition is provided by the summary in the specification at line 22 of page 8 through line 3 of page 9. Therefore, independent claims 16 and 18 are submitted to clearly distinguish patentably over the art. Dependent claims 17 and 19 depend from and further define independent claims 16 and 18 in terms of features of the invention described in the summary at lines 12-25 of page 11 of the specification, with respect to the second embodiment. Therefore, such claims are also submitted to clearly distinguish patentably over the art.

Also enclosed is an Information Disclosure Statement (IDS) being filed in order to make of record certain references cited in an office action which has just issued in connection with the corresponding Korean application. The IDS includes copies of the Korean office action and an English translation thereof, the 2 Japanese applications cited in the office action and English language abstracts thereof, and U.S. Patent No. 5,910,891 which corresponds to one of the Japanese applications.

In conclusion, claims 1-15 and new claims 16-19 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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